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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: James Digby Collier et al.

Title: INTEGRATED CIRCUIT

Docket No.: 491.039US1

Filed: April 3, 2000

Examiner: Unknown



Serial No.: 09/541,857

Due Date: N/A

Group Art Unit: 2811

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the attached:

- Communication Re: Incorrect Filing Receipt (1 pg.)
- Copy of Filing Receipt (1 pg.)
- A return postcard.
- Other: A copy of the first page of the application as filed. (1 pg.)

No Additional fee is required.

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described above, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 28 day of June, 2000.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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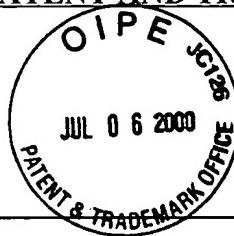
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S/N 09/541,857

PATENT

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COMMUNICATION RE: INCORRECT FILING RECEIPT

Commissioner for Patents
Washington, D.C. 20231

Applicants hereby request correction of the Filing Receipt with respect to the above-identified patent application. In the Filing Receipt received June 12, 2000, (copy enclosed), the title is misspelled. It reads: Integrtated circuit. It should read: **Integrated circuit**, as evidenced in the first page of the application as filed (copy enclosed).

Applicants would appreciate the above-identified printing error be corrected and that a new "corrected" filing receipt be sent to Applicants' representatives at the address given below.

Respectfully submitted,

JAMES DIGBY COLLIER ET AL.

By their Representatives,

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Date June 28, 2000

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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/541,857	04/03/2000	2811	0	491.039US1	7	37	3

21186
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N/A

Date Mailed: 06/09/2000

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the PTO processes the reply to the Notice, the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

James Digby Collier, Cambridge, UNITED KINGDOM;
 Ian Michael Sabberton, Cambridge, UNITED KINGDOM;

Continuing Data as Claimed by Applicant

THIS APPLICATION IS A CON OF PCT/GB98/02963 10/02/1998

Foreign Applications

UNITED KINGDOM 9721082.7 03/10/1997

If Required, Foreign Filing License Granted 06/08/2000

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Title

Integtrated circuit

Schwegman, Lunberg,
Woessner & Kluth, P.A.

JUN 12 2000

Preliminary Class

257

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Data entry by : MEREDITH, WANDA

Team : OIPE

Date: 06/09/2000





INTEGRATED CIRCUIT

The present invention relates to a semiconductor integrated circuit and more particularly to a CMOS or 5 similar type of circuit when used in a frequency divider circuit ("pre-scaler").

In many high frequency radio receivers a synthesiser and a voltage controlled oscillator are required to 10 generate the local carrier signal that is used to perform a first demodulation of the received high frequency radio signal. However, the synthesiser is generally unable to take the high frequency carrier signal directly as an input. Therefore a pre-scaler must be used to divide the 15 carrier frequency down to a frequency that can be accepted by the synthesiser. A pre-scaler circuit generally comprises a number of divide by 2 circuits and some control logic to provide, for example, a divide by 16 or 17 circuit. Each divide by 2 circuit generally 20 comprises a pair of latch circuits connected in a master slave configuration.

In a conventional CMOS latch circuit capable of lower frequency operation, a signal on the data input is passed through to the output while the clock signal is 25 high. When the clock signal goes low the latch maintains the same output until the clock signal goes high again, when a new data value is allowed through. The conventional CMOS latch comprises two inverters connected in series and two transmission gates. The data input 30 of the latch is connected to the input of the first inverter through one of the transmission gates. The output of the second inverter (which is also the output of the latch) is fed back to the input of the first inverter through the other transmission gate. To prevent 35 the feedback and the data input interfering with each

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